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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,488	02/26/2004	Puneet Gupta	YOR920040091US1	4982
33233	7590 11/28/2005		EXAMINER	
LAW OFFICE OF CHARLES W. PETERSON, JR. 11703 BOWMAN GREEN DRIVE SUITE 100			HA, NATHAN W	
			ART UNIT	PAPER NUMBER
RESTON, V	A 20190		2814	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	T		His			
	Application No.	Applicant(s)				
Office Action Summer	10/787,488	GUPTA ET AL.				
Office Action Summary	Examiner	Art Unit				
The MANUAIC DATE of this communication and	Nathan W. Ha	2814				
The MAILING DATE of this communication app Period for Reply	lears on the cover sheet with the t	correspondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DATE of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period value to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tir will apply and will expire SIX (6) MONTHS from the cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on <u>06 Sectors</u>						
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3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 4	33 O.G. 213.				
Disposition of Claims						
4) Claim(s) 4-29 is/are pending in the application.						
4a) Of the above claim(s) is/are withdray	wn from consideration.					
5) Claim(s) 12-28 is/are allowed.						
7)⊠ Claim(s) <u>4,6 and 8-10</u> is/are objected to.	6)⊠ Claim(s) <u>5,7,11 and 29</u> is/are rejected. 7)⊠ Claim(s) <u>4.6 and 8-10 is/are objected to</u>					
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examine	r					
10) The drawing(s) filed on is/are: a) acc		Examiner.				
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correct	ion is required if the drawing(s) is ob	pjected to. See 37 CFR 1.121(d).				
11) The oath or declaration is objected to by the Ex	caminer. Note the attached Office	e Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:	priority under 35 U.S.C. § 119(a	n)-(d) or (f).				
1. Certified copies of the priority document	s have been received.					
2. Certified copies of the priority document	• •					
3. Copies of the certified copies of the prio	•	ed in this National Stage				
application from the International Bureau * See the attached detailed Office action for a list		ad				
See the attached detailed Office action for a list	of the certified copies not receive	eu.				
Attachment(s)	"□·· · -	(070, 110)				
Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948)	4) Interview Summary Paper No(s)/Mail D	oate				
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	5) Notice of Informal 6) Other:	Patent Application (PTO-152)				

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DETAILED ACTION

Claim Objections

1. Claim 29 is objected to because of the following informalities:

Claim 29 recites, "logic blocks are CMOS logic circuits, each comprising one or more field effect transistor, FETs." The limitation "each comprising one or more field effect transistors appears to be redundant and inaccurate since a CMOS circuit must be composed of only one n-MOS and only one p-MOS. Appropriate correction is required.

Claim Rejections - 35 USC § 112

- The following is a quotation of the second paragraph of 35 U.S.C. 112:
 The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claims 29 and 4-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In this case, claim 29, for example, recites limitations of the first type cell and the second type cell. However, the type of the cells is unclear since it does not specifically describe or specify a certain type of the preferred cells in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 29, 5, 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lenosky (US 2004/0208266, newly cited) in view of Kono et al. (US 2002/0030510, newly cited, hereinafter, Kono.)

In regard to claims 29 and 7, and in accordance with the 112 rejection above, in fig. 2, for example, Lenosky discloses an IC circuit including at least one combination logic path comprising a plurality of logic blocks 202-208, at least one of the logic blocks being a first type cell, A/D logic, and at least one other of the blocks being a second type cell, D/A logic. Lenosky, however, does not expressly descried the logic blocks in detail, or how they were formed. It should be noted that most logic blocks, for example, latches, flip-flops are designed by a combination of CMOS devices since CMOS is a fundamental element in any integrated circuit. A CMOS circuit provides delay and inverted outputs.

Kono, in figs. 1-10, discloses an analogous IC device including cells and logic blocks, the logic blocks further are formed by CMOS devices. See Kono's claim 17, for example.

Therefore, it would have been obvious to one of skilled in the art at the time of the invention was made to recognize the obviousness of using CMOS devices to construct an integrated circuit as taught by Kono in order to take the advantages as mentioned above.

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The above combination of Lenosky and Kono does not explicitly teach that the fabrication process of the cells (claims 29 and 7.) However, the limitation "fabrication" parameter having affect on the types of the cells" in claim 29 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

In regard to claim 5, Kono further discloses the cells or transistors are densely formed, fig. 5.

In regard to claim 11, the IC shown in Lenosky is a standard IC.

Allowable Subject Matter

6. Claims 12-28 are allowed.

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7. Claims 4, 6, 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 29, 5, 7, and 11 have been considered but are most in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Nathan Ha

November 19, 2005